IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

1. (previously presented) An abnormality detection device for detecting an abnormality in a communication bus, the device comprising:

a timer counter configured to measure a time during which a logical output of said communication bus remains at a first logical level which is a high level or a low level; and

a comparator configured to compare the time measured by said timer counter with a threshold value and to output an abnormality detection signal indicating an abnormality in said communication bus when the time surpasses said threshold value, wherein the abnormality detection device is independent of a CPU controlling the communication bus and detects the abnormality directly from the communication bus.

2. (previously presented) The abnormality detection device as claimed in claim 1, wherein said timer counter is initialized at intervals determined according to an event signal supplied thereto.

3. (original) The abnormality detection device as claimed in claim 2, comprising at least two units of said timer counter and said comparator, the timer counter in each of said units being individually initialized at said intervals.

4. (previously presented) The abnormality detection device as claimed in claim 1, further comprising:

a plurality of comparison value registers respectively configured to store a plurality of threshold values; and

a selector configured to store a threshold value from among said plurality of said threshold values according to a selection signal supplied thereto so as to supply said threshold value to said comparator.

5. (previously presented) An abnormality detection device for detecting an abnormality in a communication bus, the device comprising:

at least two timer counters each configured to measure a time during which a signal transmitted through said communication bus continues to be a first logical level;

a register configured to cumulatively add the time measured by at least one of said at least two timer counters, the register being initialized at predetermined intervals; and

a comparator configured to compare the time cumulatively added by said register with a threshold value and to output an abnormality detection signal indicating an abnormality in said communication bus when the cumulative time obtained by said register surpasses said threshold value, wherein the abnormality detection device is independent of a CPU controlling the communication bus and detects the abnormality directly from the communication bus.

6. (original) The abnormality detection device as claimed in claim 5,

wherein said register supplies said cumulative time to at least one of said at least two timer counters, and

said at least one of said at least two timer counters measures the time by using said cumulative time as an initial value.

7. (previously presented) A microcomputer connected to a communication bus, the microcomputer comprising:

a CPU configured to control the communication bus;

a timer counter configured to measure a time during which a logical output of said communication bus remains at a first logical level which is a high level or a low level; and

a comparator configured to compare the time measured by said timer counter with a threshold value and to output an abnormality detection signal indicating an abnormality in said communication bus when the time surpasses said threshold value, wherein the timer counter and the comparator are independent of the CPU and are operatively coupled to detect the abnormality directly from the communication bus.

8. (previously presented) An abnormality detection device to detect an abnormality in a communication bus, the device comprising:

at least two timer counters each configured to measure a time during which a signal transmitted through said communication bus continues to be a first logical level;

a register configured to cumulatively add the time measured by at least one of said at least two timer counters, the register being initialized at predetermined intervals; and

a comparator configured to compare the time cumulatively added by said register with a threshold value and to output an abnormality detection signal indicating an abnormality in said communication bus when the cumulative time obtained by said register surpasses said threshold value,

wherein said register supplies said cumulative time to at least one of said at least two timer counters, and

said at least one of said at least two timer counters measures the time by using said cumulative time as an initial value.

9. (previously presented) The abnormality detection device as claimed in claim 1, which detects the abnormality directly from the communication bus by hardware.

10. (previously presented) The abnormality detection device as claimed in claim 5, which detects the abnormality directly from the communication bus by hardware.

11. (previously presented) An abnormality detection device detecting an abnormality in a communication bus, comprising:

a timer counter configured to measure a time during which a logical output of said communication bus remains at a first logical level; and

a comparator configured to compare the time measured by said timer counter with a threshold value and to output a signal indicating an abnormality in said communication bus when the time surpasses said threshold value, wherein the abnormality detection device is independent of a CPU controlling the communication bus and detects the abnormality directly from the communication bus.

12. (previously presented) An abnormality detection device to detect an abnormality in a communication bus, comprising:

at least two timer counters each configured to measure a time during which a signal transmitted through said communication bus continues to be a first logical level;

a circuit configured to cumulatively add the time measured by at least one of said at least two timer counters; and

a comparator configured to compare the time cumulatively added by said circuit with a threshold value and to output an abnormality detection signal indicating an abnormality in said communication bus when the cumulative time obtained by said circuit surpasses said threshold value,

wherein said circuit supplies said cumulative time to at least one of said at least two timer counters, and

said at least one of said at least two timer counters measures the time by using said cumulative time as an initial value.